Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **GND**
2. **N. TRIGGER**
3. **OUTPUT**
4. **N. RESET**
5. **CONTROL VOLTAGE**
6. **THRESHOLD**
7. **DISCHARGE**
8. **VDD**

**.051”**

**.047”**

**DIE ID**

**20**

**555**

**6**

**7**

**8**

**5 4 3**

**2**

**3**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND or FLOAT**

**Mask Ref: 555**

**APPROVED BY: DK DIE SIZE .047” X .051” DATE: 8/17/21**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: LMC555**

**DG 10.1.2**

#### Rev B, 7/1